VC-QSFPDD-200G-SR8 (MPO16)

200Gb/s QSFP-DD SR8 Optical Transceiver

Features

- ✓ Up to 25.78Gbps data rate per channel by NRZ modulation
- ✓ Support 200GAUI-8 electrical interface
- ✓ Integrated 850nm VCSEL array and PD array
- ✓ Single MPO16 connector receptacle optical interface compliant
- ✓ DDM function implemented
- ✓ Case temperature range: 0℃ ~ +70℃
- ✓ Hot-pluggable QSFP-DD form factor
- ✓ Maximum power consumption <4W
- ✓ Single +3.3V power supply
- ✓ Reach up to 70m on MMF(OM3)
- ✓ Reach up to 100m on MMF(OM4)
- ✓ Compliant with ROHS2.0

Applications

- ✓ Data centers and Cloud Networks
- ✓ 200G Interconnect Requirements

Standards

- ✓ IEEE 802.3bs
- ✓ QSFP-DD MSA CMIS 4.0 compliant
- ✓ Compliant with ROHS2.0

Description

The AscentOptics QSFP28-DD 200G SR8 Transceiver is designed to transmit and receive

serial optical data links up to 8 x 25.87Gbps data rate by NRZ modulation format over multi-mode fiber.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{IN}	0	4	V	
Storage Temperature	T_{STG}	-40	85	C	Ambient
Relative Humidity	RH	5	85	%	

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
operating case Temperature	Top	0	-	70	C	
Power Supply Voltage	Vcc	3.14	3.3	3.46	V	
Power Supply Current	Icc	-	1000	-	mA	
Power Consumption			3.3		W	

Transmitter characteristics

Transmitter Parameter	Min	Typical	Max	Unit	Note
Signaling rate, each lane	25.78125±100ppm			Gb/s	
Lane Wavelength Range	840		860	nm	
Modulation Format	NRZ				
Average Optical Power per lane	-8.4		2.4	dBm	1
RMS Spectral width			0.6	nm	
Optical Modulation Amplitude (OMA), each lane	-6.4		3	dBm	
Average launch power of OFF transmitter, each lane			-30	dBm	
Launch Power in OMA minus TDEC, each lane	-7.3			dBm	
Transmitter and Dispersion Eye Closure, each lane			4.3	dB	
Extinction Ratio	2				
Data Input Differential Peak-to Peak Voltage Swing	20		950	mVpp	2
LOS Assert Threshold	120			mVpp	3
Optical Return Loss Tolerance			12	dB	
Transmitter Eye mask definition{X1,X2,X2,Y1,Y2,Y3}	{0.3,0.38,0.45,0.35,0.41,0.5}				

Notes:

1. Even if the TDP<0.9dB,the OMA(min) most exceed this value
2. AC coupled internally.
3. Tx Data Input Differential Peak-to-Peak Voltage Swing

Receiver Optical Specifications

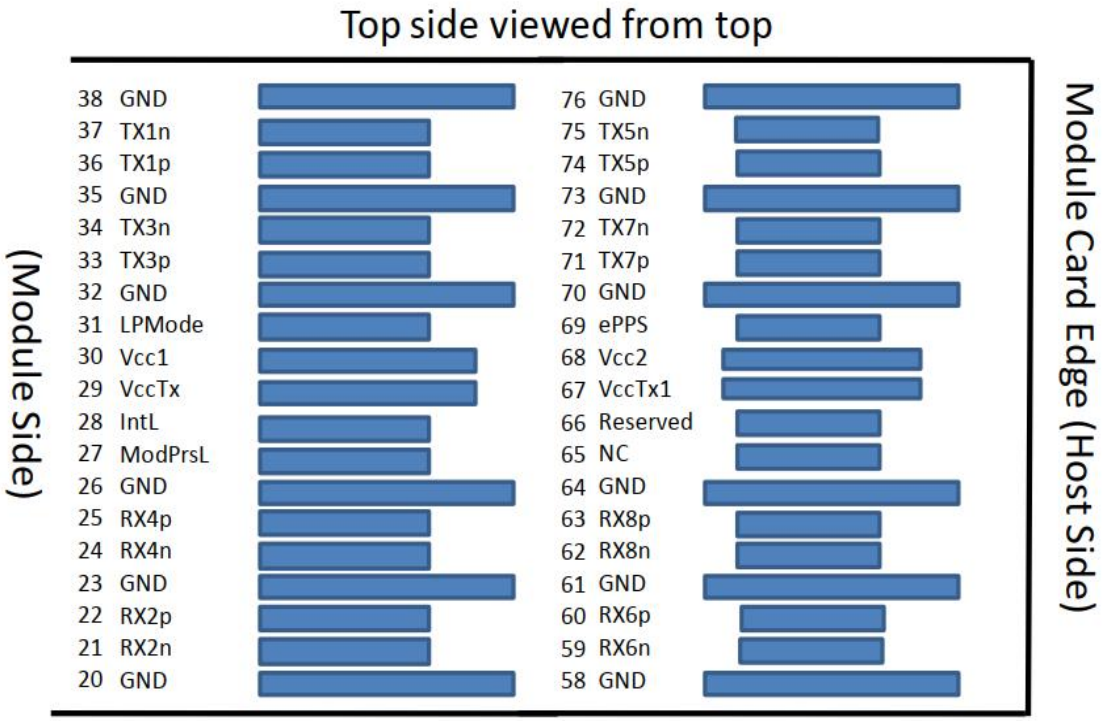
Transmitter Parameter	Min	Typical	Max	Units	Note
Signaling rate, each lane	25.78125±100ppm			Gb/s	
Lane Wavelength Range	840		860	nm	
Modulation Format	NRZ				
Damage Threshold	3.4			dBm	
Average Receive Power, each lane	-10.3		2.4	dBm	
Receiver Power, each lane (OMA)			3.0	dBm	1
Receiver Reflectance			-12.0	dB	
Stressed Receiver Sensitivity(OMA),each lane			-5.2	dBm	2
Data Output Differential Peak-to Peak Voltage Swing, each lane	300		800	mVpp	
RX_Los_Assert Min/Max	-30.0			dBm	
RX_Los_De-ASSERT Min/Max			-12.0	dBm	
RX_Los_Hysteresis	0.5			dBm	
Stresssd Receiver Eye Mask Definition{X1,X2,X2,Y1,Y2,Y3}	{0.28,0.5,0.5,0.33,0.33,0.4}				

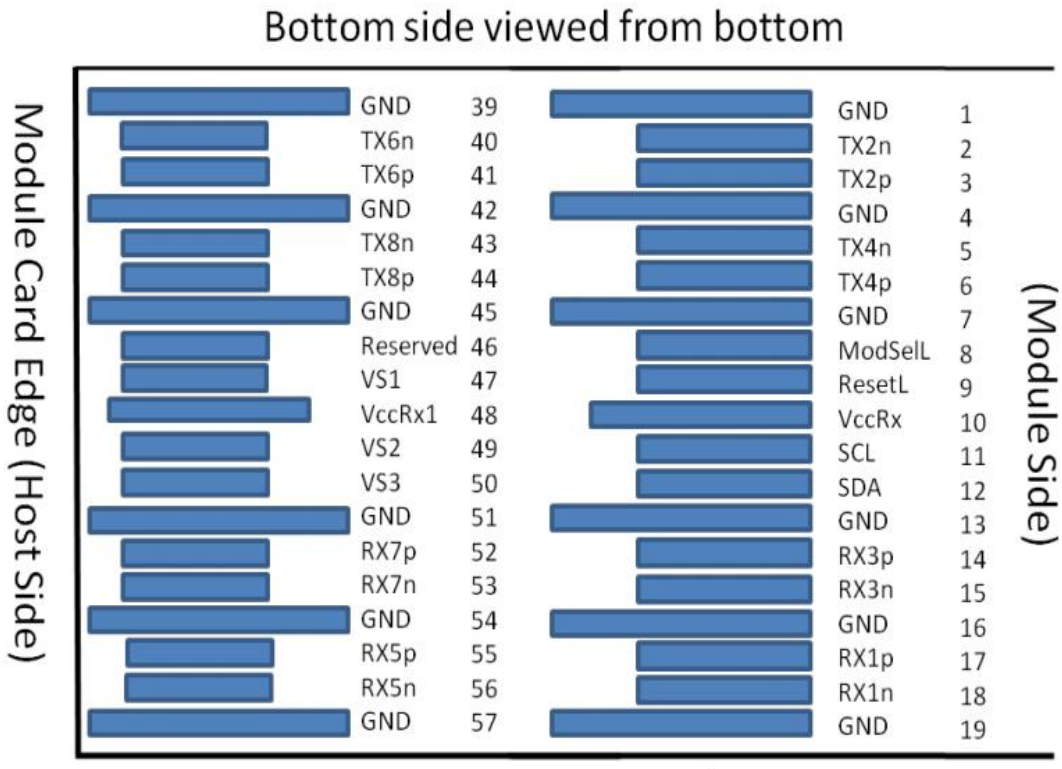
Notes:

1. Measured with 25.78125-Gbps of PRBS-31 at 5x10-5 BER.

2. AC coupled with 100ohm differential output impedance.

Electrical Connector Layout





Electrical Pin Definition - QSFP28-DD Terminal

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Electrical Pin Definition - QSFP28-DD Terminal

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

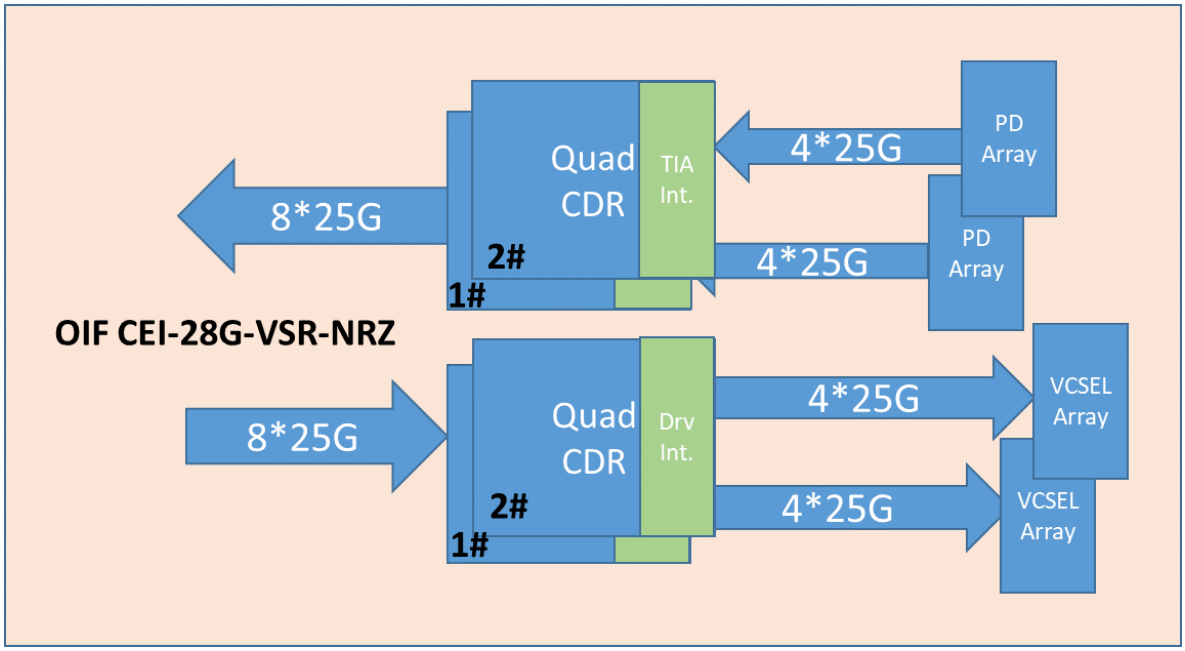
Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

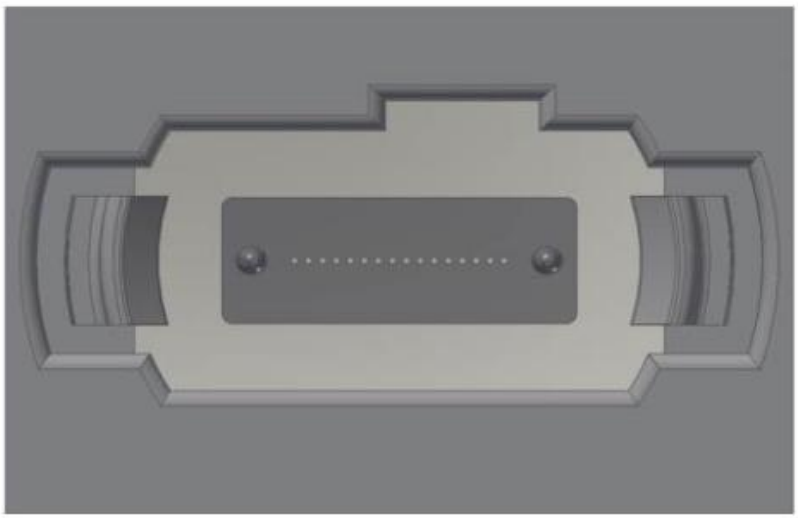
Module Block Diagram



Module Memory Map

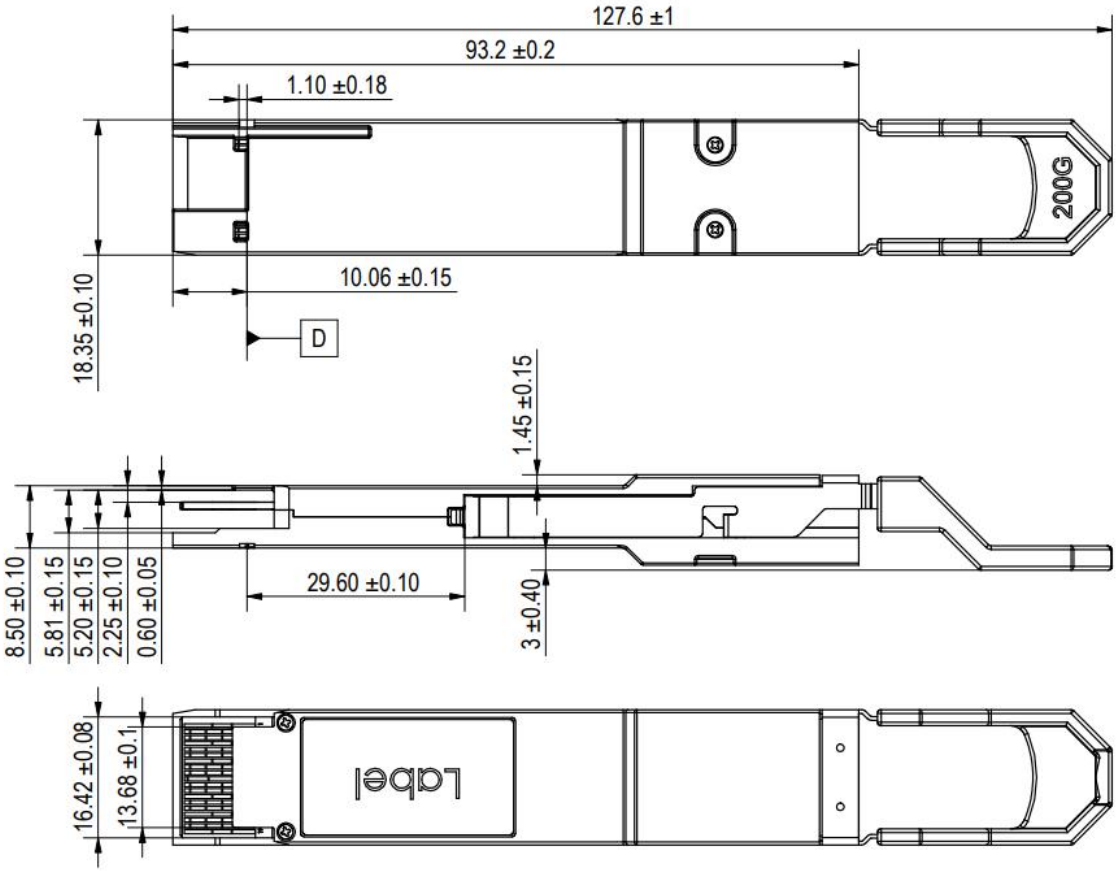
Compatible with QSFP28-DD CMIS rev 4.0

Optical interface



Package Outline

Compatible with the QSFP28-DD Type 2 Specification for pluggable form factor modules.



Ordering information

Part Number	Product Description
VC-QSFPDD-200G-SR8 (MPO16)	QSFP28-DD 200G SR8 Optical Transceiver